UNITED STATES PATENT APPLICATION

FOR

ULTRA THIN BACK-ILLUMINATED

PHOTODIODE ARRAY

STRUCTURES AND FABRICATION METHODS

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BACKGROUND OF THE INVENTION

5   1.   Field of the Invention

The present invention relates to semiconductor photodiodes, and in particular, to the structures of high performance, back-illuminated photodiode arrays and the methods of fabricating such structures.

10   2.   Prior Art

Conventional photodiode array structures are based on either front illuminated or back illuminated technologies. Figure 1a is a simplified cross section of an exemplary prior art front illuminated photodiode array and Figure 1b is a

15   simplified cross section of an exemplary prior art back illuminated photodiode array. The substrate 1 may be either n-type or p-type material, with opposite conductivity type diffused regions 2 therein. This creates a p-on-n or n-on-p structure, respectively. The anode metal pads 3 for the p-

20   on-n structure (the cathode contacts for the n-on-p structure) are always on the device front surface. The opposite polarity electrode is usually deposited (plated, sputtered, or evaporated) on the chip back side in the case

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of the front illuminated structure (see metal layer 4, Figure
1a), or is made on the device front surface (see metal pads
4, Figure 1b) using metallized through vias 6,7 in the case
of the back illuminated structure. The blanket-type

5   implantation 5 of the back surface of the die of the same
conductivity type as the substrate improves both the charge
collection efficiency and DC/AC electrical performance of the
devices.

Each of the two approaches - the front illuminated and

10   back illuminated structures - has its own advantages and
disadvantages. For example, traditional front illuminated
structures like that shown in Figure 1a allow building high
performance photodiodes and photodiode arrays, but impose
severe constraints on the metal run width. Those constraints

15   limit a design of the front illuminating photodiode array to
the use of either a smaller number of elements, or larger
gaps between adjacent elements. Note that the metal runs
should be accommodated in between adjacent diffusion areas 2
(see Figure 1a).

20   Back illuminated structures reported recently by several
companies take advantage of solder bump technology to
electrically connect elements of the array to an external
substrate or PC board using the contacts (bumps) on the front
surface of the structure. By utilizing solder bump

technology, the metal interconnects, which usually reside on top of the active surface between the adjacent elements openings, may be moved to the substrate or PC board upon which the chip is mounted. Such an approach allows

5   minimizing the gaps between adjacent elements of the array, at the same time allowing a virtually unlimited total number of elements. However, several drawbacks of the previously reported back illuminated structures limit their application:

1) First, these structures are usually fabricated

10   using relatively thick wafers (>50 µm) and the resistivity of the material has to be high enough (>1000 Ohm-cm) to deplete the entire volume at zero bias, which is required for many applications;

2) Second, the application of a high resistivity

15   material usually diminishes the photodiode performance with respect to the leakage current and shunt resistance;

3) Third, if a high resistivity material is not used, then the time response will be very long (micro

20   seconds or even longer) because the time response would be determined by the diffusion processes rather than drift processes of the totally depleted structures;

4) Fourth, there are little or no structural features that isolate adjacent cells from each other within the entire thickness of the device, which results in relatively high cross-talk, especially at zero bias.

5   Summarizing, such parameters as the leakage current, shunt resistance, cross-talk, spectral sensitivity, and temporal response are of main concern for the prior art of back illuminated structures. Additionally, the handling of thin wafers (<50 μm thickness) in the wafer fabrication

10   process is a matter of great concern by itself, and would become increasingly important with the further decrease of the wafer thickness.

BRIEF DESCRIPTION OF THE DRAWINGS

The main ideas of the invention are demonstrated by the accompanying drawings, in which:

Figures 1a and 1b are schematic cross sections of
5 typical, conventional prior art structures for the front illuminated photodiode arrays and back illuminated photodiode arrays, respectively.

Figure 2 is a schematic cross section of an ultra thin, back illuminating photodiode array in accordance with the
10 present invention.

Figure 3 is a schematic cross section of a sample structure of the present invention having a 30μm thick, n-type Silicon wafer.

Figure 4a through 4c illustrate sequential steps of a
15 method for fabricating electrodes of a thin wafer photodiode array structure in accordance with the present invention.

Figure 5 illustrates an exemplary layout of cathode and anode pads across the front surface of the wafer.

Figure 6 is a cross section taken through one of the
20 metal contacts of Figure 5.

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DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The objectives of the present invention include:

1) To provide a multiple element, back side illuminated 2D-photodiode array with a superior performance of all
5   elements;

2) To provide a fabrication method for the back side-illuminated photodiode array on an ultra thin wafer.

It is therefore an object of this invention to provide a structure for silicon multi-element, 2-D photodiode arrays
10   having greatly improved characteristics over prior art arrays, making it useful in such applications as CT scanner applications, etc.

Another object is to provide a method of fabricating Si devices on ultra thin wafers, which method can be suitable
15   for fabrication of flip-chip, multi-element, 2-dimensional arrays of silicon photodiodes.

These and other objects of the present invention will become apparent from the following disclosure. In this disclosure, first preferred embodiments of finished diode
20   arrays will be described, and then the preferred method of fabricating the arrays will be described.

Figure 2 is a simplified cross-sectional view of a semiconductor ultra-thin chip photodiode array in accordance with a preferred embodiment of the present invention. The structure is built using either n-type or p-type bulk silicon

5   1. For brevity, the anode in the case of p-on-n structure or the cathode in the case of n-on-p structure will be referred to as "the first electrode", while the cathode in the case of p-on-n structure and the anode in the case of n-on-p structure will be referred to as "the second electrode."

10   The material resistivity, thickness of the wafer/die, dopants concentrations and doses, and diffusion conditions are preferably chosen to satisfy the following requirements:

        a) The active area (the first electrode) diffusion
        2 extends sufficiently close to the back surface of the
15   finished die that the rest of the volume between the
        diffusion edge and the blanket implant in the die back
        surface and part of the blanket implant, the space
        indicated as "d" in the Figure 2, becomes completely
        depleted at a zero volt bias;

20   b) The uniform, "blanket" type implantation 5 of
        the back side of the wafer with the implant of the same
        polarity as the one of the majority carriers of the
        wafer bulk 1 provides excellent majority carrier
        conductivity across the wafer back side; and ensures a

vertical electric field for carrier collection beneath the first electrode to minimize cross talk;

c) The second electrode, diffusion 8, is applied from the front surface of the wafer using the implantation and drive protocols that allow for the diffusion to reach the wafer back side, overlapping thereby with the blanket implantation 5 and providing perfect electrical contacts between the second electrode network across the entire wafer. At the same time, an oxide layer 12 is grown on the front surface, shown in Figure 6, but not shown in the earlier Figures for clarity in the illustrations of the doped regions.

An example of a real structure built using a n-type bulk Si with the resistivity of approximately 400 ohm-cm is shown schematically in Figure 3. At a zero bias, the width of a depletion region is approximately 9μm and extends up to and into (but not through) the blanket implantation 5 in the wafer back side. (See the hatched with dots area 9 in Figure 3. The blanket diffusion 5 is only approximately 0.6μm thick, so the depletion region extends approximately to, but not quite all the way to, the wafer back side.) The built-in potential creates an electric field across the depletion region and facilitates rapid collection of non-equilibrium carriers created by light near the back surface of the die.

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The non-equilibrium carriers have no or very little

possibility of being collected by the electrodes from

adjacent cells because:

The electric field near the die back surface, where

5   the carriers photo-generation predominantly occurs is

directed perpendicular to the die surface; therefore,

the carriers move (drift) primarily toward the junction

of the same cell, having almost no possibility of being

trapped by an adjacent cell;

10   The second electrode diffusion region 8, which is

n+ diffusion in the case of Figure 3, spans the entire

thickness of the die and acts as an effective carrier

isolator from adjacent cells.

The first electrode diffusion 2 may overlap with the

15   second electrode diffusion 8 close to the front surface of

the die as shown in Figure 3. This overlapping may

significantly decrease the breakdown voltage, which is not

important for a zero bias device.

Thus, exemplary representative diffusion profiles of the

20   first electrode 2 and second electrode 8 are shown in Figure

3. The depth of the first electrode diffusion 2 should be

less than the finished substrate thickness (typically less

than 50 μm, and more typically approximately 30 μm as shown

in Figure 3) by an amount that approximately equals the depletion depth for the substrate material 1 at zero bias. The second electrode diffusion 8 should span the entire thickness of the substrate, or at least to a sufficient depth

5   to provide a reliable low resistance contact with the blanket implantation 5 of the back side of the wafer. Note that the dopants 5 and 8 are of the same polarity.

Such a structure may be fabricated starting with a thicker substrate (for example 300 μm) for structural

10   stiffness and integrity during the processing, using three masking steps:

First, as shown in Figure 4a, the second electrode 8 implantation/diffusion is applied followed by a drive. At this stage, the difference in the

15   final diffusion depths for the first electrodes 2 and second electrodes 8 (approximately 9μm) is formed.

Second, as shown in Figure 4b, the first electrode 2 implantation/diffusion is applied followed by a drive. By the end of this stage, the diffusion

20   profiles 2 and 8 almost reach their final configuration.

Third, as shown in Figure 4c, the second electrode 8 receives an additional enhancement

followed by a drive to ensure superior electrical contacts and to activate dopants. At this stage, the profiles of both the cathode and anode diffusions reach their final configurations (see the solid lines

5   and hatched areas in Figure 4c). The diffusion profiles prior to this third step of dopants implantation/diffusion/drive are shown schematically with the dashed lines in Figure 4c. The future back surface of the wafer after back side grinding and

10   polishing is shown schematically with the dashed line 10.

The array is then reduced in thickness by grinding the back side of the array, preferably to provide a substrate thickness of under approximately 50 μm, and more preferably

15   to approximately 30 μm. The final thickness achieved, of course, is preferably selected in accordance with the resistivity of the substrate and the depth of the first electrode diffusion so that the diffusion is spaced away form the back side of the substrate an amount that approximately

20   equals the depletion depth for the substrate material at zero bias. Then a blanket implant of the first conductivity type is made to the back side of the wafer, which implant improves both the charge collection efficiency and DC/AC electrical performance of the photodiode arrays. Activation of the

25   implant does not significantly alter the first and second

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electrode diffusions. Alternatively, a diffusion for the back side could be used if desired. The blanket implant is quite thin compared to the depletion region, with the depletion region extending into, but not through, the blanket

5   implant in the final array.

An ideal flatness of the back side surface of the die is very important for many applications, e.g., for CT scanners that require attaching of a scintillator crystal to the back side of the photodiode array. To help satisfy this

10   requirement, the oxide layer 12 is evenly patterned and the metal pads 14 contacting the first electrode 2 and second electrode 8 are evenly spaced across the surface of the die 16 and made the same size to provide identical ball bumping conditions throughout the wafer (see Figures 5 and 6). The

15   oxide layer 12 and metal pads 14 are represented by the larger diameter circles in Figure 5, with the smaller diameter circles describing the contact openings.

The present invention photodiode arrays exhibit very low cross talk because of the excellent isolation of each pixel.

20   Also, because of the small depletion volume, the arrays exhibit low noise and low temperature sensitivity. When used in X-ray systems, they exhibit low radiation damage, and have thermal characteristics similar to scintillators to which they will are mounted. The technique of using a deep

diffusion in conjunction with a thin substrate for making

electrical contact to the back side of the substrate may, of

course be used in other semiconductor devices. While the

deep diffusion in the preferred embodiment is of the same

5   conductivity type as the substrate, this is not a limitation

of the invention, as the deep diffusion may be of the

opposite conductivity type, if desired.

While preferred exemplary embodiments of the present

invention have been disclosed herein, such disclosure is only

10   for purposes of understanding the exemplary embodiments and

not by way of limitation of the invention. It will be

obvious to those skilled in the art that various changes in

fabrication process and structure of the photodiode arrays

may be made without departing from the spirit and scope of

15   the invention, as set out in the full scope of the following

claims.